

09487497 110398
855077 46748760

14. A semiconductor wafer comprising:
a Si substrate;
a plurality of components positioned on the Si
substrate, and each pair of neighboring
5 components having a shallow trench between them
for isolating the two components;
a dielectric material filled in each shallow trench
for electrically isolating the two components on
two sides of the shallow trench;
10 wherein for shallow trenches with widths greater
than a predetermined size, at least one dummy is
generated at the bottom of each of the shallow
trenches to form a plurality of new shallow
trenches with widths less than the predetermined
15 size, and the dielectric material filled in each
of the shallow trenches covers above each dummy
to achieve electrical isolation.
15. The shallow trench isolation method of claim 14
20 wherein the predetermined size for the chosen
shallow trenches is 2 μm .
16. The shallow trench isolation method of claim 14
wherein the preferred height of any dummy is around
25 300 \AA to 500 \AA .
17. The semiconductor wafer of claim 14 wherein each
dummy is formed of Si, and the method for forming
the shallow trenches and the dummies on the
30 semiconductor wafer comprises:
performing a photolithography and etching method on
the surface of the semiconductor wafer down to
at least the Si substrate to make the shallow

09187197 110398

trenches between each component;
applying photoresist to each dummy's position at the
bottom of each shallow trench which is wider than
the predetermined size;
5 etching all the shallow trenches on the surface of
the semiconductor wafer again to complete all the
shallow trenches and the dummies; and
stripping off the photoresists on the semiconductor
wafer.

10
18. The semiconductor wafer of claim 14 wherein the
method for forming all the shallow trenches and
dummies comprises:
using a photomask to define the positions of all the
15 shallow trenches and dummies on the surface of
the semiconductor wafer; and
performing a photolithography and etching method to
form the shallow trenches and dummies
simultaneously.

20
19. The semiconductor wafer of claim 18 wherein when
performing the photolithography and etching method,
the semiconductor wafer is covered with a
photoresist layer, and the photomask contains a
25 plurality of transparent areas with different
light penetration capability for defining the
positions of all the shallow trenches and the
dummies on the semiconductor wafer so that the
amount of light emitted through the photomask to the
30 photoresist layer over each shallow trench's
position is different from the amount of light
emitted to each dummy's position whereby all the
shallow trenches and the dummies can be formed at

the same time by using the photomask and the photoresist layer.

add
Bp

09187197 110398